Electronic Version
Stylesheet Version v1.1.1

# SINGLE POLY EMBEDDED EPROM

## Abstract

A novel structure of nonvolatile memory is disclosed. The non-volatile memory includes two serially connected PMOS transistors. The characteristic of the devices is that bias is not necessary to apply to the floating gate during the programming mode. Thus, the control gate is omitted for the structure or layout, thereby saving the space for making the control gate. The carrier may be "automatically injected" into floating gate for programming the status of the devices.